

Evaluating TMR Techniques in the Presence of Single Event Upsets

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Benefits of SRAM FPGAs in Space

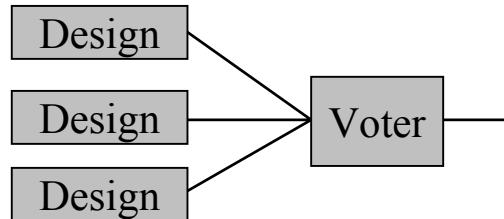
- FPGAs Can Be customized To Application-Specific Algorithms
 - Customizable datapath for application specific computations
 - Often faster and more efficient than a programmable processor
- FPGAs Are Reprogrammable
 - Configuration after the spacecraft has been launched
 - FPGA resources can be used for multiple instruments, missions, or changing spacecraft objectives
 - Errors in an FPGA design can be repaired while in orbit

Single-Event Effects of SRAM FPGAs

- Static memory sensitive to single-event upsets (SEU)
- Large amount of static memory in FPGAs
 - Configuration memory
 - User memory and flip-flops
- Upsets within the configuration memory may *modify* the behavior of the design
 - Internal Logic and Interconnect
 - Global clocking and configuration modes
 - Operation of Input/Output pads
- Design redundancy necessary for proper operation

SEU Mitigation Through TMR

- Tripple Modular Redundancy (TMR)
 - Triplicate circuit of interest
 - Vote on circuit output (majority voter)



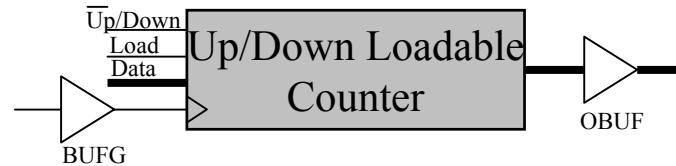
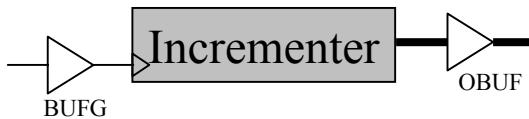
- TMR masks all single failures in design
- Goal: investigate the effectiveness of TMR on FPGAs

TMR Evaluation Approach

- Measure the number of “sensitive” configuration bits
 - Number of configuration bits that effect the operation of the design
 - Measured using the BYU SEU Simulator
- Apply a form of TMR to design under test
- Measure the configuration sensitivity of TMR
- Measure cost of TMR: area (LUTs), speed (MHz)

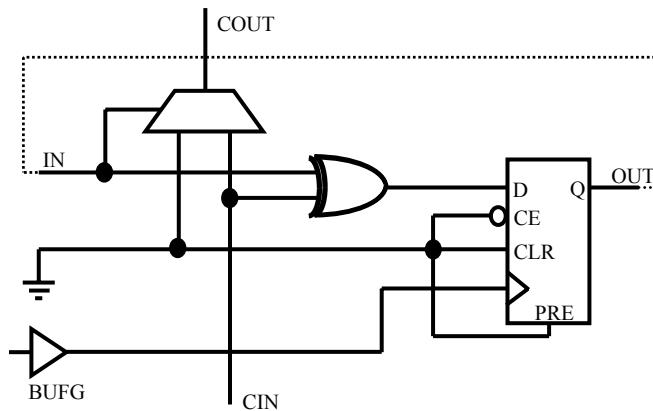
Counter Designs

- 8-bit Incrementer
 - 8 LUTs
 - 220 MHz
 - 446 Sensitive Bits
- 8-bit up/down loadable counter
 - 10 LUTs
 - 220 MHz
 - 463 Sensitive Bits

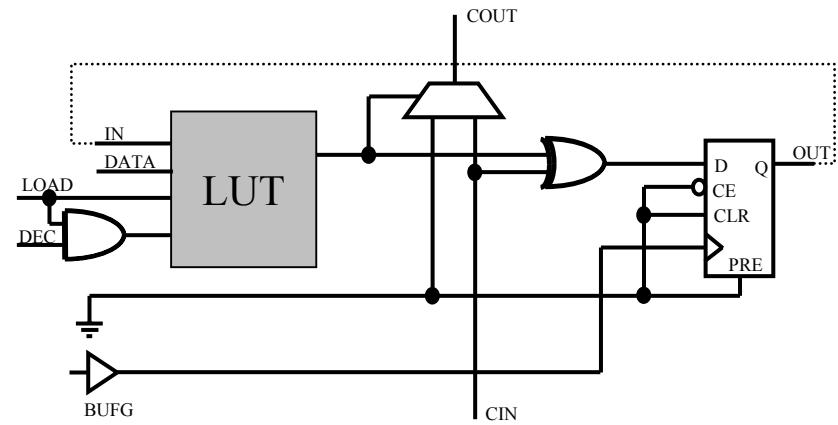


Internal Counter Designs (1 bit)

Simple Counter



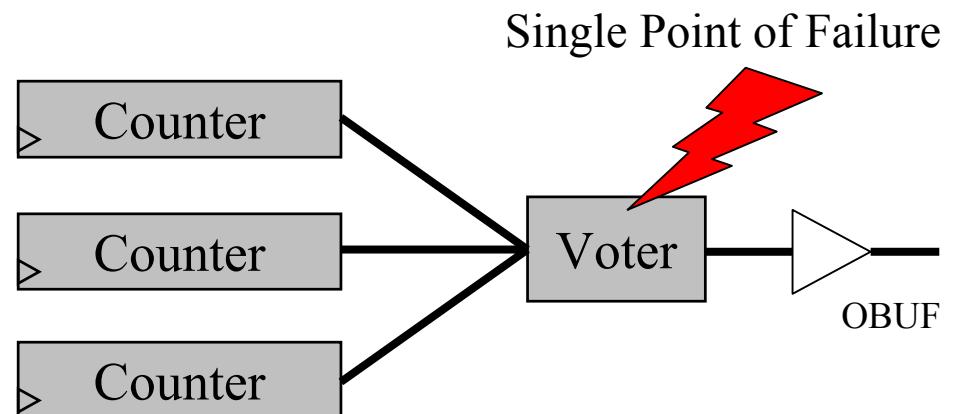
Up/Down Loadable Counter



TMR Techniques

- TMR with 1 Voter

- Single point of failure in the voter
- Useful only when voter size is small relative to the rest of the circuit



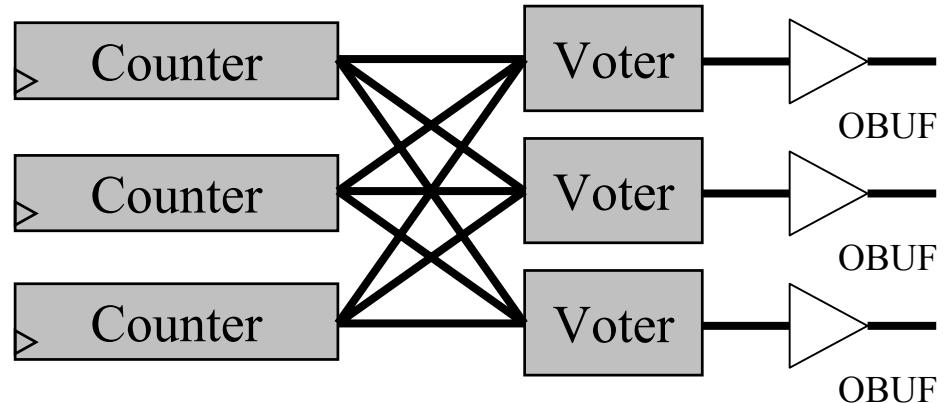
Incrementer

Up/Down counter

	LUTs	Failures	Speed (MHz)	LUTs	Failures	Speed (MHz)
No Redundancy	8	446	220	10	463	220
TMR 1 Voter	35	410	217	41	484	217

TMR Techniques

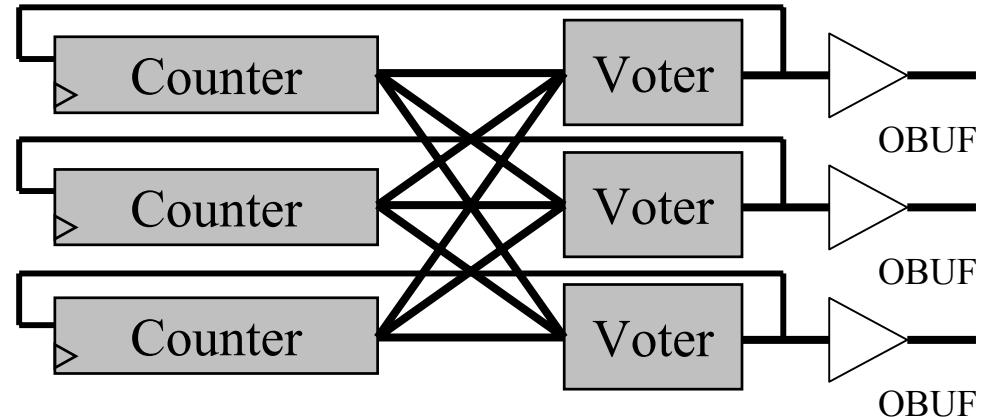
- TMR with 3 Voters
 - More LUTs required
 - Reliability increases



	Incrementer			Up/Down counter		
	LUTs	Failures	Speed (MHz)	LUTs	Failures	Speed (MHz)
No Redundancy	8	446	220	10	463	220
TMR 1 Voter	35	410	217	41	484	217
TMR 3 Voters	51	89	199	57	36	213

TMR Techniques

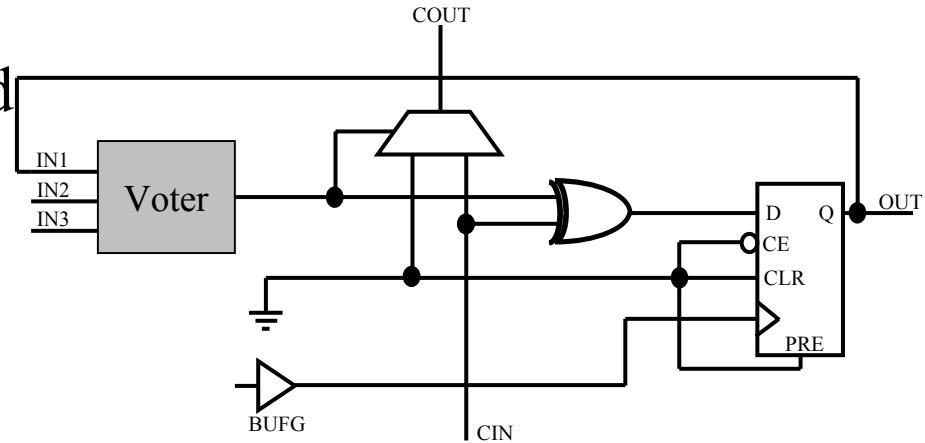
- Feedback TMR
 - Prevents synchronization errors
 - Improved reliability
 - Operates at slower speed



	Incrementer			Up/Down counter		
	LUTs	Failures	Speed (MHz)	LUTs	Failures	Speed (MHz)
No Redundancy	8	446	220	10	463	220
TMR 1 Voter	35	410	217	41	484	217
TMR 3 Voters	51	89	199	57	36	213
Feedback TMR	51	14	160	57	15	157

Merging Voter With Logic

- Logic Resources can be reduced by merging voter with logic
- 1-Bit incrementer with TMR requires only 1 LUT



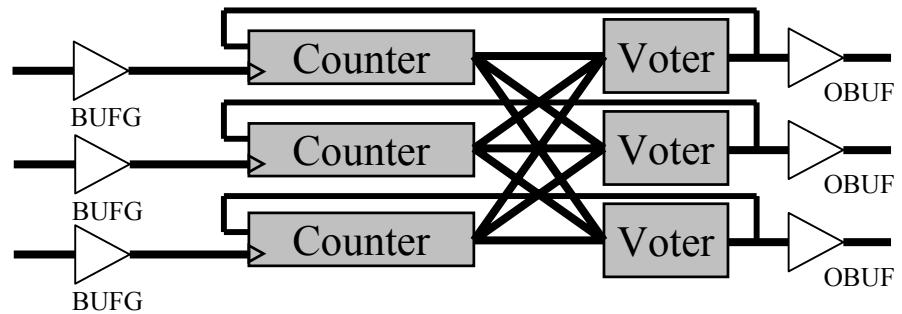
Incrementer

Up/Down counter

	LUTs	Failures	Speed (MHz)	LUTs	Failures	Speed (MHz)
No Redundancy	8	446	220	10	463	220
TMR 1 Voter	35	410	217	41	484	217
TMR 3 Voters	51	89	199	57	36	213
Feedback TMR	51	14	160	57	15	157
Mapped Feedback	27	15	194	N/A	N/A	N/A

Tripling Clocks

- Single point of failure in clock domain
- Error free operation requires three clocks
- Feedback TMR and 3 clocks provides bulletproof design

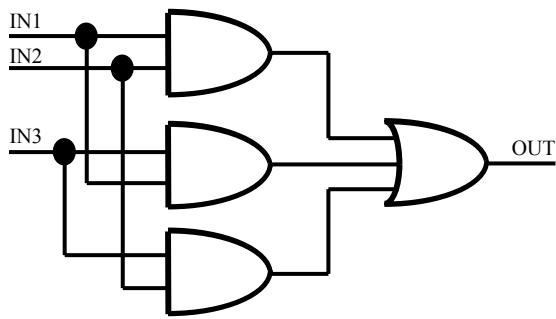


	Incrementer			Up/Down counter		
	LUTs	Failures	Speed (MHz)	LUTs	Failures	Speed (MHz)
No Redundancy	8	446	220	10	463	220
TMR 3 Voters	35	99	201	41	37	217
Feedback	51	0	167	57	0	158
Mapped Feedback	27	0	204	N/A	N/A	N/A

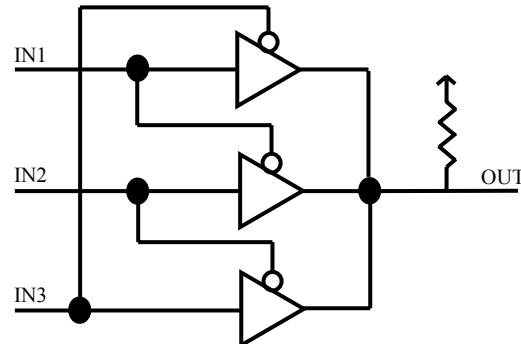
No Failures with Feedback TMR & 3 clocks!

LUT vs. TBUF Voters

LUT Voter



TBUF Voter



- 1 LUT per bit

- no LUTs required
- 3 TBUFs per bit
- runs slower than LUT voter

TBUF Voters

Incrementer

Up/Down counter

	LUTs	Failures	Speed (MHz)	LUTs	Failures	Speed (MHz)
TMR 1 Voter	27	293	217	33	425	212
TMR 3 Voters	27	30	219	33	32	213
Feedback TMR	27	19	106	33	14	102
Map Feedback	27	19	105	N/A	N/A	N/A

Single Clock w/TBUF Voters

Incrementer

Up/Down counter

	LUTs	Failures	Speed (MHz)	LUTs	Failures	Speed (MHz)
TMR 3 Voters	27	46	219	33	40	215
Feedback TMR	27	0	123	33	0	117
Map Feedback	27	0	123	N/A	N/A	N/A

Triple Clocks w/TBUF Voters

Summary

- Bulletproof counter design is possible with feedback TMR and triplicated clocks
 - Simple incrementer (free voters)
 - Area cost: ~3x Speed cost: runs ~7% slower
 - Up/down loadable counter
 - Area cost: ~6x Speed cost: runs ~30% slower
- Bulletproof counter is possible with TBUF voters
 - Area cost: ~3x Speed cost: runs ~50% slower

Conclusions

- It is possible to completely mitigate against configuration upsets for the two counter designs
- TMR requires significant resources and may reduce the speed of the design
- Future Work
 - Investigate additional architecture structures
 - Identify increase of power due to TMR